disclaimer and Claims 9, 10, 25-29, 36, and 45 have been amended without the introduction of any new matter.

The outstanding Official Action presents an objection to Claims 28-33 and 46 under 35 U.S.C. §132, a rejection of these claims under the first paragraph of 35 U.S.C. §112 as including prohibited new matter, a rejection of Claims 9-11, 14, 15, 24-29, 34-45, and 49-53 under 35 U.S.C. §103(a) as being unpatentable over Rogers et al. (U.S. Patent No. 4,571,819, Rogers) in view of Lee et al (U.S. Patent No. 4,952,524, Lee), and a rejection of Claims 47 and 48 under 35 U.S.C. §103(a) as being unpatentable over Rogers in view of Lee in further view of Hunter et al. (U.S. Patent No. 4,631,803, Hunter).

The Advisory Action mailed February 13, 2002, suggested that the clearly improper objection to Claims 28-33 and 46 under 35 U.S.C. §132 and corresponding rejection of these claims under the first paragraph of 35 U.S.C. §112 were being maintained even though the objection conflicted with the MPEP and the rejection was in conflict with established case law requirements. In this regard, the Request for Reconsideration filed on January 18, 2002, pointed out errors as to the objection and rejection that were not treated in the Advisory Action as follows:

> The objection to Claims 28-33 and 46 under 35 U.S.C. §132 and the corresponding rejection of Claims 28-33 and 46 under the first paragraph of 35 U.S.C. §112 are both traversed because they have no basis in law or fact.
>
> First of all, MPEP §2163.01 cautions that it is error to object to claims under 35 U.S.C. §132 in light of In re Rasmussen, 650 F.2d 1212, 211 USPQ 323 (CCPA 1981) which holds that new matter objections can only be properly made as to ~~amendments to the abstract, specification, or drawings.~~ Thus, MPEP §2163.01 instructs examiners that claims are not to be objected ~~to under 35 U.S.C. §132, instructions that have been ignored in terms of the~~ present erroneous objection to Claims 28-33 and 46. under 35 U.S.C. §132. Accordingly, it is believed that this erroneous objection should be withdrawn.
>
> Besides the fact that the objection under 35 U.S.C. §132 to Claims 28-33 and 46 violates the PTO's own guidelines, it is further clearly without merit for the reasons presented below as to traversing the corresponding

rejection of Claims 28-33 and 46 under the first paragraph of 35 U.S.C. §112.

In this regard, the outstanding Office Action appears to have committed further error in basing this rejection on the exact claim language not appearing in the specification as filed with respect to the language added by the amendment to these claims made on June 13, 2001, that states that the "oxide films are deposited [as in Claims 31 and 46, or "buried" as in Claims 32 and 33] in the grooves so as not to include any nitride film in the grooves" or the requirement for "depositing oxide film directly on the thin thermal oxidation films" set forth by Claims 28 and 29. However, as further explained in the PTO's own guidelines of MPEP §2163 (at page 2100-161of August 2001 revision):

> An applicant may show possession of an invention by disclosure of drawings or structural chemical formulas that are sufficiently detailed to show that applicant had possession of the claimed invention as a whole. See, e.g., *Vas-Cath*, 935F.2d at 1565, 19 USPQ2d at 118 ("drawings alone may provide a "written description" of an invention as required by Sec. 112\"); *In re Wolfensperger*, 302 F.2d 950, 133 USPQ 537 (CCPA1962) ("the drawings of applicant's specification provide sufficient written descriptive support for the claimed invention at issue); *Autogiro Co. Of America v. United States*, 384 F.2d 391, 398, 155 USPQ 697, 703 (Ct. Cl. (1967) ("In those instances where a visual representation can flesh out words, drawings may be used in the same manner and with the same limitations as the specification.") ... .

Thus, the present rejection of Claims 28-33 and 46 under the first paragraph of 35 U.S.C. §112 is in error in that it ignores the clear written descriptive support that is present in the showings of Figs. 3A-E, for example, with respect to the language added by the amendment made on June 13, 2001, requiring that "oxide films are deposited [as in Claims 31 and 46, or "buried" as in Claims 32 and 33] in the grooves so as not to include any nitride film in the grooves" or the requirement for "depositing oxide film directly on the thin thermal oxidation films" set forth by Claims 28 and 29. In this respect, the absence of "any nitride film in the grooves" and the fact that the illustrated oxide film "is directly on the thin thermal oxidation films" could not be any clearer.

> Besides improperly ignoring Figs.3A-E, for example, the outstanding Office Action ignores the specification description of the deposit of the oxide films 71 in the groove 6 at page 6, lines 3-15, for example. Moreover, even though the Examiner notes that page 19, line 26 suggests that a Si_3N_4 layer may be grown, the fact that a substitute thermal oxidation film can be used or that both of these alternatives can be omitted under the teachings of the paragraph beginning at line 22 of page 19 has been erroneously ignored. In this

regard, "may" is not a synonym for "must," it is a permissive term well understood to only indicate possibilities, not absolutes. Thus, Page 19, lines 24-26, instruct the artisan that omit both the thin thermal oxidation film and the Si3N4 film can be omitted as part of the invention, not that either or both must be included. This is particularly true in light of Figs. 3A-3E that show the case where an oxide film is directly deposited on the inner wall of the groove. Accordingly, as there is clear support in the application as filed, the rejection of Claims 28, 29, 30-33 and 46 under the first paragraph of 35 U.S.C. §112 is traversed as these claims are clearly directed to one of the optional choices available as described in the application..

In addition to the traversal of this erroneous objection and erroneous rejection applied to Claims 28-33 and 46, the Request for Reconsideration filed on January 18, 2002, included the following relevant brief summary of background information as follows:

Before considering the obviousness rejections, it is believed that some background information would be helpful. One of the feature of the present invention pertaining to a method of manufacturing a semiconductor substrate having STI regions and a device region sandwiched by the STI regions lies in the method such that oxide film buried in the groove by an organic silicon based CVD method does not to generate any crystal defects around the grooves.

Trench isolation is relatively old, and various requirements such as uniformity, planarization, step coverage, film quality, low temperature in process, and the like are known limitations imposed relative thereto. In particular, step coverage and low temperature in process are recognized as being important. In manufacturing a miniaturized semiconductor device having groove width narrower than 1μ, which is required more and more for high integration density, with further miniaturization to the width of less than 0.5μ being sought after, a low temperature insulating film with high quality is required.

High Temperature Oxide (HTO) CVD techniques using monosilane (SiH4), N2O, etc. grown at 600-900 °C have been tried as the filler for STI grooves. However, HTO films require relatively high temperature processing and provide poor step coverage. Thus, doped glass, such as phosphosilicate glass (PSG) or orboro-phosphosilicate glass (BPSG) has been used to lower the melting point of such HTO films, and a reflow-process used to planarize the surface at temperature of 950-1150üÄ. However, it is very difficult to completely fill the narrow groove having width less than 1μ used for VSLI isolation, because of the known problem of the generation of voids. Therefore, HTO CVD and reflow-process are applied to relatively large geometry trench isolations having grooves with width larger than 5μ.

In response to the lower temperature processing requirement, a Low Temperature Oxide (LTO) CVD technique using SiH4 and N2O, etc. grown at a relatively low temperature of 300-450 °C has also been tried. However LTO film has poor step coverage, is inferior in film quality, and because it exhibits tensile stress, it has poor small crack immunity.

Recently, an "organic silicon based CVD method" has been tried to provide a filler for a narrow groove having width less than 1μ. Here the term "organic silicon based CVD method" means a CVD method using an organic silicon material such as TEOS (Tetraethylorthosilicate; Si(OC2H5)4), TMOS(Tetramethoxysilane; Si(OCH3)4), TPOS (Tetrapropoxysilane; Si(OC3H7)4), or DADBS (Diacetoxyditertiarybutoxysilane; (C4H9O).2 Si--(OCOCH3).2) as the source material. Such an organic silicon based oxide film has excellent step coverage and can be grown at a temperature of 450-750 °C, or less depending on the source materials employed. However, such organic silicon based oxide films formed by an "organic silicon based CVD method" were found to have several drawbacks due to stress in the organic silicon based oxide films due to shrinkage caused by dissociation of moisture inherently contained in the organic silicon source material that causes crystalline defects around the grooves having a width narrower than 1μ. Such crystal defects cause serious failures relative to miniaturized STI configuration which even more desirably encompass grooves having a width narrower than 0.5μ.

Applicants observations as to the deficiencies in the films produced by the above-noted methods of manufacturing a semiconductor substrate having STI regions encompassing narrower width grooves and the need to suppress/decrease crystal defects around the grooves that led to filling STI grooves using the organic silicon based CVD method of the present invention. To that end, the method of the present invention embraces (a) forming a plurality of grooves on part of a surface of the semiconductor substrate; (b) depositing oxide films in the grooves by an organic silicon based CVD method; (c) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and (d) annealing the oxide films, after said removing, at a substrate temperature which is greater than or equal to 1150 °C but less than or equal to 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}. By employing the method of the present invention, the stress in the buried oxide films is relaxed, and the generation of crystal defects is suppressed as disclosed, for example, in FIG.4.

The Request for Reconsideration filed on January 18, 2002, included the following relevant arguments as to the prior art rejections that were not responded to. As these

arguments remain unanswered, they are repeated as follows:

With regard to the rejection of Claims 9-11, 14, 15, 24-29, 34-45, and 49-53 under 35 U.S.C. §103(a) as being unpatentable over Rogers in view of Lee, it is clear that Rogers has no disclosure or suggestion of the claimed step of depositing oxide films in the grooves using an organic silicon based CVD method. Although Rogers may teach a step of outgassing phosphorus or boron dopant from the doped trench oxide 19 at a temperature of about 1,000-1,200 °C (see column 3, lines 63-68 and column 6, lines 62-65), this outgassing phosphorus or boron dopant cannot be reasonably said to correspond to the claimed step of annealing organic silicon based oxide films at a substrate temperature greater than or equal to 1150 °C but less than or equal to 1350 °C. This is because the phosphorus or boron doped trench oxide 19 of Rogers that is buried in the groove is clearly different from the claimed organic silicon based oxide films.

In this last respect, there are many kinds of silicon oxide films that are known to greatly differ depending on the method used to form them, such as thermal oxide, HTO, LTO, Spin-On-Glass (SOG), sputtered oxide, vacuum evaporated oxide, anodic oxidized oxide, etc. These films formed by these different methods have different melting points, different etching rates (See Fig.7B, for example), different dielectric constants, different crystallographic structures, different Raman spectrums (See Fig.7A for example), etc., although they are represented by exactly the same notation of SiO_2. Annealing conditions for these different films also are different and each one must be determined by its chemical properties, its physical properties, and its crystallographic structures, respectively. The artisan is well aware of such considerations and would not use the same annealing conditions for such differently formed oxides at least because of their different melting points.

Moreover, considering defects generated in claimed device region in a vicinity of the grooves, the crystallographic structures of such differently formed oxides also play very important roles, because the stress induced at the interfaces between the buried materials and the semiconductor substrate depends on the crystallographic structures of the buried oxides. Therefore, it is unreasonable to assume that the artisan would have any reason to believe that the outgassing of dopant condition for the doped trench oxide 19 of Rogers, or the annealing conditions for an HTO for that matter, would be used if the oxide films in the grooves were formed by depositing these oxide films in the grooves by using an organic silicon based CVD method as the independent claims require.

Moreover, in light of the above discussion, the assertion in the outstanding Action that "since the annealing temperature of Rogers et al is within the claimed range, therefore, the dislocation density in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2} is clearly not well founded as it is confusing the oxides of entirely different properties materials and making the entirely conjectural assumption that no

matter how an oxide is formed, it will respond exactly in the same manner when exposed to the same heating conditions. Consideration of the differences in melting point alone belie this improper conjectural assumption.

Furthermore, Rogers teaches a very complicated structure including a stress relief oxide layer 16 with a thickness of about 30 to 100 nm, contacting the sidewall of the groove, a polycrystalline silicon etch-stop layer 17 with a thickness of about 100 to 300 nm on the stress relief oxide layer 16, a silicon nitride barrier layer 18 with a thickness of 100 to 250 nm on the polysilicon layer 17 and finally the doped silicon dioxide glass layer 19 on the silicon nitride barrier layer 18. Such a complicated structure is inherently required in Rogers, since it employs the doped silicon dioxide glass layer 19. However, the layered sub-structures buried in the groove play very important roles as to defining the dislocation density in the device region, because the stress induced at the interfaces between the buried materials and the semiconductor substrate depends on the crystallographic structures associated with this composite stacked structure. Clearly, in such complicated layered structure having four different films in the groove, the stress at the interfaces between the buried materials and the semiconductor substrate is a matter of speculation. Again, the conjectural assumption that the outgassing of Rogers will inherently result in the claimed dislocation density is clearly without merit.

Furthermore, although Column 6, lines 36-40 of Rogers sates "It should be noted that one of the advantages of the present process is its adaptability to a wide range of trench dimensions, e.g., trench widths of 1μm to 50μm", Column 3, lines 40-44 sates "Optionally for relatively wide trenches (typically those wider than 5μm), a polymer such as PMMA (polymethylmethacylate) may be formed on the dielectric after the reflow step to facilitate forming a smooth outer surface topology of the complete wafer." Claim 15 also states "wherein the trench width is greater than or equal to approximately 5 μm." In view of these disclosure, Rogers et al is directed to old devices having relatively large dimensions such that the width of groove is larger than 5μm. Rogers is silent as to suggesting any truly miniaturized structure. Clearly, as the stress relief oxide layer 16 must have the thickness of about 30 to 100 nm, the polycrystalline silicon etch-stop layer 17 must have the thickness of about 100 to 300 nm, and the silicon nitride barrier layer 18 must have the thickness of 100 to 250 nm to appropriately provide the functions of the respective layers, such as blocking the diffusion of dopant from the doped silicon dioxide glass layer 19, the width of groove cannot be miniaturized. In such large-scale devices like that of Rogers, the claimed dislocation in the device region in a vicinity of the groove will not play an important role, and it is sure that Rogers did not look for or observe such kind of crystal defects. Therefore, the Examiner's assertion that "since the annealing temperature of Rogers et al is within the claimed range, therefore, the dislocation density in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}" is again without merit.

Furthermore, the proposed combination of Lee and Rogers is clearly without merit because of the differences in the oxide materials and the methods of forming them. As noted above, simply because different oxide materials may be represented by same notation of SiO_2 this does not mean they have common properties or that they are interchangeable. In this respect, col. 5, lines 10-16, state that BPTEOS is annealed at temperature of 850-950°C for ½ to 2 hours or at temperature of 1000 °C for 30-60 sec. However, BPTEOS cannot be annealed at elevated temperature of 1000-1200 °C for 2 to 8 hours, which is the outgassing condition of the phosphorus or boron dopant from the doped trench oxide 19 in Rogers. With such higher temperature of 1000-1200 °C, boron dopant and phosphorus dopant contained in BPTEOS film 25 will diffuse into semiconductor substrate 11, penetrating the diffusion barrier 21 and the stress-relief layer 23, to finally deteriorate seriously the device performance. BPTEOS film 25 contains 3 % boron and 3 % phosphorus dopant (See col. 4, lines 28-31). Different materials must be annealed in different way considering the chemical and physical properties of the respective materials.

In view of present rejection against Claims 9-11,14,15 and 24 under 35 U.S.C. §103(a) relying upon Rogers in view of Lee being improper for the above noted reasons, it is respectfully requested that this rejection withdrawn.

Similarly, the rejection against Claim 24-29 34-45 and 47-53 under 35 U.S.C. §103(a) in view of the combination of Lee and Rogers with or without Hunter is clearly improper and respectfully requested to be withdrawn as Hunter cures none of the deficiencies noted as to Lee and Rogers .

In addition to these traversals of the rejections of Claims 9-11,14,15, 24-29, and 34-53, it is noted that the rejection of Claim 47 is now moot as this claim has been canceled. Also, the rejections under 35 U.S.C. §103(a) are further believed to not apply to the presently amended claims because Rogers has no disclosure or suggestion of claimed step of depositing oxide films using the claimed non doped organic silicon source. Instead, Rogers teaches the step of outgassing the phosphorus or boron dopant from the doped trench oxide 19-19 at a temperature of about 1,000-1,200 degrees C (See column 3, lines 63-68 and column 6, lines 62-65). And, as noted above, Rogers teaches a very complicated structure including a stress relief oxide layer 16 with a thickness of about 30 to 100 nm in contact with the sidewall of the groove, a polycrystalline silicon etch-stop layer 17 with a thickness of about 100 to 300 nm on the stress relief oxide layer 16, a silicon nitride barrier layer 18 with

a thickness of 100 to 250 nm on the polysilicon layer 17 and finally the doped silicon dioxide glass layer 19 on the silicon nitride barrier layer 18. Such complicated structure is inherently required in Rogers, since it uses the doped silicon dioxide glass layer 19.

Furthermore, Rogers fail to the show claimed step of forming a plurality of grooves having a width narrower than 0.5μm. This is because the above-noted stress relief oxide layer 16 must have a thickness of about 30 to 100 nm, the polycrystalline silicon etch-stop layer 17 must have a thickness of about 100 to 300 nm, and the silicon nitride barrier layer 18 must have a thickness of 100 to 250 nm to appropriately provide the functions of the respective layers, such as blocking the diffusion of dopant from the doped silicon dioxide glass layer 19. Therefore, if these layers are to function properly they must be provided in the indicated widths and the width of the grooves cannot be narrower than 0.5μm.

Lee further has no disclosure or suggestion of the claimed step of depositing oxide films using the claimed non doped organic silicon source. Column 5, lines 10-16, of Lee states that BPTEOS is annealed at temperature of 850-950°C for ½ to 2 hours or at temperature of 1000°C for 30-60 sec. The BPTEOS film 25 contains 3 % boron and 3 % phosphorus dopant (See column 4, lines 28-31). BPTEOS cannot be annealed at the elevated temperature of 1000-1200°C for 2 to 8 hours, which is the outgassing condition of the phosphorus or boron dopant from the doped trench oxide 19-19 in Rogers.

Therefore, the proposed combination of Lee and Rogers is clearly without merit as using the Rogers higher temperature of 1000-1200°C would cause boron dopant and phosphorus dopant contained in BPTEOS film 25 of Lee diffuse into the semiconductor substrate 11, penetrating the diffusion barrier 21 and the stress-relief layer 23, which would seriously reduce device performance. Before a *prima facie* case of obviousness can be said to exist, it must be clear that there is a reasonably expectation of success (see In re Vaeck, 20

USPQ2d 1438, 1442 (Fed. Cir. 1991)) and the PTO must establish a reasonable basis as to why the artisan would have been led to combine these references (see In re Lee, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002) and In re Dembiczak, 506 USPQ 614, 617 (Fed. Cir. 1999)). The present rejections fail to meet both these criteria.

As no further issues are believed to remain outstanding in this application, it is believed that this application is clearly in a condition for formal allowance and an early and favorable action to this effect is, therefore, respectfully requested.

Respectfully submitted,

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Please amend the claims as follows:

9. (Four times amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and a device region sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate, each of grooves having a width narrower than 0.5μm;

(b) depositing oxide films in the grooves by [an organic silicon based] a CVD method using a non doped organic silicon source;

(c) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(d) annealing the oxide films, after said removing, at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}.

10. (Twice amended) The method of claim 9, wherein the [organic silicon based] CVD method is any of atmospheric pressure CVD method, low pressure CVD method, plasma CVD method, photo CVD method, and liquid phase CVD method.

25.(Thrice amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation regions and device regions sandwiched by the shallow trench

isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate, each of grooves having a width narrower than 0.5μm;

(b) depositing oxide films in the grooves by [an organic silicon based] a CVD method using a non doped organic silicon source;

(c) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so the dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than 1 μm^{-2}; and

(d) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

26. (Thrice amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate, each of grooves having a width narrower than 0.5μm;

(b) burying oxide films in the grooves by [an organic silicon based] a CVD method using a non doped organic silicon source; and

(c) annealing said oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, and an etching rate by ammonium fluoride solution of said oxide films is less than 130 nm/min, which is substantially identical to that of a thermal oxide film.

27. (Thrice amended) A method of manufacturing a semiconductor substrate having

a shallow trench isolation, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate, each of grooves having a width narrower than 0.5μm;

(b) burying oxide films in the grooves by [an organic silicon based] a CVD method using a non doped organic silicon source; and

(c) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C, but less than or equal to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, the respective predetermined rates of the ring structures are determined according to rates of integrated Raman intensities corresponding to respective ring structures to a total integrated Raman intensity, and the structures are formed to satisfy either of or both conditions that said higher order ring structures are substantially more than 85 % of an overall structure and said lower order ring structures are substantially less than 15 % of the overall structure.

28. (Thrice amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by [an organic silicon based] a CVD method using a non doped organic silicon source;

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a

corresponding device region; and

(e) annealing the oxide films, after said removing, at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}.

29. (Thrice amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by [an organic silicon based] a CVD method using a non doped organic silicon source;

(d) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than 1 μm^{-2}; and

(e) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

36. (Amended) A method for forming a microelectronic structure, the method comprising:

(a) forming a mask layer on a substrate wherein the mask layer exposes a part of the substrate;

(b) forming a groove in the exposed part of the substrate

(c) depositing a layer of an insulating film using a non doped source so as to fill the

groove and cover the mask layer;

(d) annealing said insulating film at a temperature which is greater than or equal to 1150°C but less than or equal to 1350°C.

45. (Amended) The method of claim 44, wherein said depositing the insulating material comprises forming an oxide by [chemical vapor deposition] a CVD method using the non doped source.

47 (Canceled).